CLAIMS:

1. A data processing apparatus, comprising:

- a plurality of data processing units (10a-b), each having an address output (14, 15) and a data input and/or output (12, 13);

- a plurality of memory units (18a,b), each having an address input and a data input and/or output;

- a switching unit (16, 17) comprising:

- first selectable connections between the data input and/or outputs (12, 13) of the processing units (10a) and selectable ones of the data input and/or outputs of the memory units (18a,b),

- second selectable connections from the address outputs of the processing units (10b) to the address inputs of selectable ones of the memory units (18a,b),

- a detection unit (20a, 30, 32) coupled to the address outputs of the processing units (10a,b), arranged to detect repetitions of a period of an address pattern output by the at least one of the processing units (10a,b),

- a state holding element (22a, 34) for controlling the first and second selectable connections, the state holding element (22a, 34) having an input coupled to the detection unit (20a, 30, 32), in order to switch the first and second selectable connections in response to the detection of a new one of said repetitions, so that identical addresses from the data processing units (10a,b) alternately map to different ones of the memory units (18a,b) during successive repetitions.

2. A data processing apparatus according to Claim 1, wherein a criterion for detecting the new one of the repetitions is programmable under the control of a program executed by the apparatus.

3. A data processing apparatus according to Claim 1, wherein the detection unit comprises an address comparator (20a) arranged to detect whether addresses from the address output of a first one of the data processing units (10a,b) fall in a range of one or more addresses associated with the memory units (18a,b), and to generate a detection signal

indicating the new one of said repetitions each time when one of the addresses from the address output of the first one of the data processing (10a,b) units has output addresses in said range a certain number of times.

4. A data processing apparatus according to Claim 3, wherein said certain number is one, and wherein said range is a subset of one or more of the addresses associated with the memory units (18a,b).

5. A data processing apparatus according to Claim 3, wherein said certain number is greater than one, the apparatus comprising a counter for counting a counted number of the addresses from the address output of the first one of the data processing units in said range at least until said certain number.

6. A data processing apparatus according to Claim 1, wherein the detection unit comprises an access memory (30) for the at least one of the data processing units (10a,b) the access memory (30) comprising locations for a plurality of the addresses that address locations in the memory units (18a,b) that are addressable by the first one of the data processing units (10a,b), the access memory (30) being arranged to record access to the locations in the memory units (18a,b), the detection unit (32) being arranged to generate a detection signal indicating the new repetition in dependence on whether the access memory (30) indicates that an address supplied by the first one of the processing units (10a,b) has been supplied before during the repetition.

7. A data processing apparatus according to Claim 6, wherein the detection unit (32) generates the detection signal when the at least one of the data processing units (10a,b) outputs an address for which the access memory (30) has previously recorded access after a previous detection of said new repetition.

8. A data processing apparatus according to Claim 6, wherein the detection unit (32) generates the detection signal when the at least one of the data processing units (10a,b) has executed more than a certain number of addresses for which the access memory indicates that the address has not been supplied previously during the repetition.

9. A data processing unit according to Claim 1, wherein said plurality of memory units (18a,b) comprises three or more memory units, the state holding element controlling the switching of the first and second selectable connections, so that identical addresses from the data processing units cyclically map to different ones of three or more of the memory units during successive repetitions.

10. A data processing unit according to Claim 1, wherein the detection unit is arranged to perform the detection of repetitions involving repetition of read and/or write control signals from at least one of the processing units (10a,b).

11. A data processing method, the method comprising:

- detecting repetition of periods of access address patterns output from at least one of a plurality of processing units
- switching selectable connections between the data input and/or outputs of the processing units and the data input and/or outputs of selectable ones of a plurality of memory units, so that a same addresses from at least one of the plurality of processing units alternately addresses a location in different ones of the memory units in dependence on the detection of said repetition.